DEMODULATOR FOR DIGITAL RADIO COMMUNICATION

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Abstract of **JP11098205**

PROBLEM TO BE SOLVED: To simplify the configuration by converting a frequency-modulated or phase-modulated signal into an intermediate frequency signal and sampling an output of a counter means operated by a prescribed reference clock, based on a reception signal with an intermediate frequency so as to detect and demodulate phase information, thereby eliminating the need for controlling sign discrimination criterion for each information transmission period. SOLUTION: A sampling means 5 is made up of an amplitude limit means 10 that limits an amplitude of the intermediate frequency reception signal outputted from a frequency conversion means 3 and a latch means 21. The latch means 21 is realized by, e.g. a D-type flip-flop 22, its D input terminal connects to an output terminal of a counter means 8, and its CLK input terminal connects to an output terminal of the amplitude control means 10. The D-type flip-flop 22 latches data in m-bit which are phase information of the intermediate frequency reception signal outputted from the counter means 8 at each leading edge of an output signal of the amplitude limit means 10.